CLAIMS

What is claimed is:

1. A semiconductor packaging device comprising:

a carrier having at least a cavity thereon;

at least a chip having a back surface and an active surface, wherein said chip is affixed to said cavity to expose said active surface, and said active surface has a plurality of first bonding pads;

a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads and via said first insulating layer;

a multi-layer structure on said first insulating layer, said multi-layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, and a second insulating layer and a plurality of exposed ball pads thereon, wherein said first plating through holes are electrically connected with said conductive layout lines, said second plating through holes, and said exposed ball pads; and

a plurality of solder balls affixed to said ball pads.

2. The semiconductor packaging device of claim 1, wherein said carrier is made of a material selected from groups of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or

combination of above.

3. The semiconductor packaging device of claim 1, wherein said carrier comprises a substrate with a circuit layer that said substrate is selected from the groups of ceramic substrate, an organic substrate, or combination of above.

4. The semiconductor packaging device of claim 1, wherein said ball pads are distributed at a location selected from the groups of above said chip, above surrounding of said chip, or combination of above.

5. A semiconductor packaging device comprising:

a carrier having at least a slot via said carrier;

at least a chip having a back surface and an active surface, wherein said chip is affixed to said slot to expose said active surface, and said active surface has a plurality of first bonding pads;

a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads and via said first insulating layer;

a multi-layer structure on said first insulating layer, said multi-layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, and a second insulating layer and a plurality of exposed ball pads thereon, wherein

said first plating through holes are electrically connected with said conductive layout lines, said second plating through holes, and said exposed ball pads; and

a plurality of solder balls affixed to said ball pads.

6. The semiconductor packaging device of claim 5, wherein said carrier is made of a material selected from groups of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

7. The semiconductor packaging device of claim 5, wherein said carrier comprises a substrate with a circuit layer that said substrate is selected from the groups of ceramic substrate, an organic substrate, or combination of above.

8. The semiconductor packaging device of claim 5, wherein said ball pads are distributed at a location selected from the groups of above said chip, above surrounding of said chip, or combination of above.

9. A semiconductor packaging device comprising:

a carrier having a circuit layout therein, a first surface with a plurality of ball pads, and a second surface with a cavity thereon and a plurality of first bonding pads;

at least a chip having a back surface and an active surface

with a plurality of second bonding pads thereon, wherein said chip is affixed to said cavity to expose said active surface;

a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads, said second bonding pads, and said first plating through holes via said first insulating layer;

a multi-layer structure on said first insulating layer, said multi-layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, wherein said conductive layout lines, said second plating through holes are connected to said first plating through holes and electrically connected to said ball pads; and

a plurality of solder balls affixed to said ball pads.

10.The semiconductor packaging device of claim 9, wherein said carrier comprises a substrate selected from the groups of ceramic substrate, an organic substrate, or combination of above.

11. A semiconductor packaging device comprising:

a carrier having a circuit layout therein, a first surface with a plurality of ball pads, and a second surface with a slot via said carrier and a plurality of first bonding pads;

at least a chip having a back surface and an active surface with a plurality of second bonding pads thereon, wherein said chip is

affixed to said slot to expose said active surface on said second surface and expose said back surface on said first surface;

a first insulating layer on said active surface and said carrier, said first insulating layer comprising a plurality of first plating through holes connected to first bonding pads, said second bonding pads, and said first plating through holes via said first insulating layer;

a multi-layer structure on said first insulating layer, said multi-layer structure comprising a plurality of conductive layout lines, a plurality of second plating through holes therein, wherein said conductive layout lines, said second plating through holes are connected to said first plating through holes and electrically connected to said ball pads; and

a plurality of solder balls affixed to said ball pads.

12.The semiconductor packaging device of claim 11, wherein said carrier comprises a substrate selected from the groups of ceramic substrate, an organic substrate, or combination of above.